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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/798,600 | 03/10/2004 | Rohit Natarajan | 42P17960 | 6358 |

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| EXAMINER | |
|---|---|
| THOMAS, SHANE M | |
| ART UNIT | PAPER NUMBER |
| 2186 | |

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/798,600 | NATARAJAN, ROHIT | |
| | Examiner | Art Unit | |
| | Shane M. Thomas | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office action is responsive to the application filed 3/10/2004. Claims 1-21 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

### *Specification*

The disclosure is objected to because of the following informalities:

It is noted that a Summary of the Invention section has not been included within the specification.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

### Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

***Claim Objections***

Claims 2 and 9 are objected to because of the following informalities:

As per claim 2, the term --the next sequential bank-- should be amended to --a next sequential bank-- as the former term has not been previously defined in the claim scope.

As per claim 9, the term --map-- should be removed from line 4 for clarification purposes. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2,7, and 14-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2, 7, and 14, it is not clear in what respect the designated bank is --sequential-- (i.e. it being the "next sequential bank) as the term is open to multiple interpretations. For one, a --sequential-- bank could imply the next bank that is accessed base on a command subsequent to a previous commend (e.g. a previous command accessed a bank and the bank to be accessed by the next command is the next "sequential" bank). Alternatively, a --sequential-- bank could imply that the next bank to be accessed is physically sequential in relation to the previous bank (e.g. bank 1 of 4 is accessed according to an associated command's address bits and the next "sequential" bank to be accessed is then bank 2). Nonetheless, for the purposes of examination, the Examiner has considered the term the --next sequential bank-- according to the first interpretation above.

As per claims 20 and 21, it is not clear whether the term --the memory module-- refers to --the memory device--, to a memory module that comprises the memory device (as claimed in claim 9), or to another (e.g. undefined) module, as --*the* memory module-- lacks proper antecedent basis. Nonetheless, for the purposes of examination, the Examiner has considered the term in accordance with claim 9 (where the memory module comprises the memory device of the integrated circuit).

Claims 15-19 are rejected as being dependent upon a rejected base claim.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 6-10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 6-10 are directed to a computer readable medium including a data signal embodied in a carrier wave (¶54 of Applicant's specification as originally filed). This subject matter does not fall within a statutory category of invention because it is neither a process, machine, manufacture, nor a composition of matter. Instead, it is directed to a form of energy. Forms of energy do not fall within a statutory category since they are clearly not a series of steps or acts to constitute a machine, not a tangible physical article or object which is some form of matter to be a product and constitute a manufacture, and not a composition of two or more substances to constitute a composition of matter.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,6-8,14,15, and 18, are rejected under 35 U.S.C. 102(b) as being anticipated by Prouty et al. (U.S. Patent No. 6,470,433).

As per claim 1, Prouty teaches an integrated circuit (figure 5 plus the connected DRAMs which are not shown) having N queues (read queues 508 and 512 and write queues 510 and 514) to receive commands [6/34-37] for a memory device (DRAM - figure 1, not shown) having M banks - four in this case [8/50-52]. The N queues having a first 508 and second 510 queue map to a first bank (either queue 508 or 510 can map to any of the four banks - [5/41-44] and [6/37-46] and are therefore mapped to the first bank - bank 0 - of the DRAM, as commands may be sent from the queues to the first bank). Prouty further teaches logic to:

(1) determine a last type (e.g. write or read) of command de-queued (so as to limit read-to-write and write-to-read transitions - it can be seen that in order to limit these transitions, logic to determine if the previous command was a write or read is necessary);

(2) determine a bank designated to receive a next command to be de-queued (a designation is stored with the command in the queues as taught in [5/41-44], [6/42-46], and [8/66 - 9/7]);

(3) inspect the first and second queues for a type of a command matching the last type of command de-queued (see [7/29-41] - as the system of Prouty minimizes r-w and w-r transitions,

and therefore after the de-queuing of the last command of a group [7/8-16], [7/52-67], it is seen that to maintain these transitions the queues would therefore be searched for a same command type as the last command de-queued);

(4) de-queue the command [7/56-60] that matches the last type of command de-queued - an inherent step as such a step would have been made if a same type of command was found in the queues 508 and 510 as the last command since the system minimizes w-r and r-w transitions [7/36-39]; and

(5) send the de-queued command to the designated bank [8/30 - 9/7], as each command has an associated bank associated therewith [5/56-65].

As per claim 2, based on the determination that is made by the memory controller of figure 5 as to which group of commands to next de-queue [7/29-41], the Examiner is considering that bank that is accessed by the subsequent group of commands to be the *next sequential bank* as it is the next bank to be accessed by the memory controller with the next command de-queued.

As per claims 3,8, and 15, Prouty teaches four additional queues are possible [7/17-22], thus combining the four queues 504-514 taught in the embodiment of figure 5, Prouty teaches a total of eight queue. Using the same logic as discussed in the rejection for claim 1, because commands from any of the queues can contain commands that may access any of the four banks of the system memory (e.g. the queues do not distinguish between bank addressed [5/56 - 6/46]), it can be seen that all eight queues are mapped to all four memory banks. Therefore, it follows that the N queues may include a third queue and a fourth queue to map to a second bank (e.g. bank 1 - [8/50-52]), which consequentially is mapped to the other banks as well as discussed, a

fifth queue and a sixth queue to map to a third bank (e.g. bank 2), and a seventh queue and an eighth queue to map to a fourth bank (e.g. bank 3).

As per claim 6, the rejection follows the rejection for claim 1 set forth supra. Additionally, Prouty teaches an inherent article of manufacturer comprising a machine-access medium included data (instructions of figures 16A-D). Such elements are inherent since it is well known in the art that a computer readable medium is required by a processor to implement the process that comprises the instruction code of figure 16A-D. Refer to [9/7-14].

As per claim 7, Prouty teaches determining the last bank to receive a command (during the last command's execution, the system of figure 5 determined which bank to receive the command by the command's corresponding bank/column and bank/row address [6/20-46]) and sending the de-queue command to a next sequential bank (based on the determination that is made by the memory controller of figure 5 as to which group of commands to next de-queue [7/29-41], the Examiner is considering that bank that is accessed by the subsequent group of commands to be the *next sequential bank* as it is the next bank to be accessed by the memory controller with the next command de-queued).

As per claim 14, the rejection of lines 1-9 and 11-15 follows the rejection of claim 1 set forth above. The rejection of lines 9-10 follows the rejection of claim 2 set forth above.

As per claim 18, Prouty teaches logic to determine the memory device includes four banks (in order to allocate as many skew 534 and active/inactive 535 registers) - [8/61-65].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pouty et al. (U.S. Patent No. 6,470,433) in view of Garrett, Jr. et al. (U.S. Patent No. 6,839,266).

As per claims 11, the rejection of lines 1-11 follows the rejection of claim 1 set forth supra. Regarding lines 12-13, Prouty teaches a DRAM receiving de-queued commands (figure 5) but does not specifically teach the well-known concept of DRAM banks being comprised on a DIMM. Garrett teaches the conventional concept of DIMMs comprising DRAMs [1/58-65]; therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the system of Prouty with the teaching of DIMMs comprising DRAM of Jarrett in order to have connected the DRAM of Prouty to the system shown in figure 5 by means of a conventional memory slot to allow for beneficial elements such as the ease of upgrading (switching out the present DRAM with a DIMM having more DRAM banks stored thereon) - [8/61-65]) or the like.

As per claim 12, Garrett teaches the DIMM (10 figure 1 of Garrett) being a single-sided memory module. As shown in figure 1, the 18 DRAM banks are all shown being on a single side of the DIMM module.

Claims 4,5,9,10,13,16,17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prouty et al. (U.S. Patent No. 6,470,433), as applied to claim 11 above, in further view of LaBerge (U.S. Patent Application Publication No. 2004/0193777).

As per claim 13, modified Prouty does not specifically teach the DIMM being multiple-sided. LaBerge teaches in ¶5 that it is advantageous to use memory comprising multiple ranks (such as multiple-sided DIMMs) so that different internal banks and rows on different memory devices (modules) can be open at the same time. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the DRAM command scheduling system of modified Prouty with the teaching of multiple-sided DIMMs of LaBerge in order to have been able to access multiple banks and rows on different modules concurrently in the system of modified Prouty, thereby allowing increasing the speed at which the system of modified Prouty executes commands to the DIMM.

As per claims 4,5,9,10,16, and 17, using the same logic as discussed in the rejection for claims 1 and 3, because commands from any of the queues can contain commands that may access any of the four banks of the system memory (e.g. the queues do not distinguish between bank addressed [5/56 - 6/46]), it would have been seen by one having ordinary skill in the art to map all of the queues (508-514 of figure 5 as well as the four additional queues discussed in Prouty [7/19-22]) to both sides of a multiple-sided DIMM in order to maintain that all banks are mapped to all of the queues (the Examiner is considering that if the number of banks remain at a constant of four, then two banks per side of the DIMM would have been implemented). Because all queues are mapped to and may send commands to any bank, it follows that the first through

fourth queues would have been mapped to a (first) side and the fourth through eighth queues would be mapped to the other side (in addition to the first side).

As per claim 19, LaBerge teaches that the system DRAM memory may be comprised of 8 banks - figure 1.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prouty et al. (U.S. Patent No. 6,470,433), as applied to claims 1-3, 6-8,14,15, and 18 above, in view of LaBerge (U.S. Patent Application Publication No. 2004/0193777) in further view of Lee (U.S. Patent No. 6,530,001).

As per claims 20 and 21, the motivation to combine Prouty and LaBerge is discussed above. Modified Prouty does not specifically teach logic used to determine whether the memory module includes one side (i.e. the memory module comprises banks on a single side of the module) or two sides (banks on both sides). Lee teaches in [4/15-44] a process for determining whether a DIMM memory module currently installed in a system is single-sided or double-sided and, based on the determination, makes a further determination regarding the bus speed of the module. Based on the speed of the module, Lee teaches disabling speed-specific clock signals associated with the DIMM. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the system of modified Prouty with the teaching of determining DIMM sides of Lee in order to have (1) allowed the system of Prouty to have been expandable to the point of being able to accept DIMMs comprising single-sided banks or double-sided banks, thereby increasing the compatibility of modified Prouty and (2) been able to determine the correct bus speed associated with the respective single or double-

sided module installed on the system of modified Prouty, thereby enabling proper communication on the memory bus between the DIMM memory and the processor accessing the data stored therein.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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